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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/713,227	11/13/2003	Hung Y. Ng	END920030086US1	1174

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SCHMEISER, OLSEN + WATTS
3 LEAR JET LANE
SUITE 201
LATHAM, NY 12110

EXAMINER	
NOVACEK, CHRISTY L	
ART UNIT	**PAPER NUMBER**
2822	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/713,227	NG ET AL.	
	Examiner	Art Unit	
	Christy L. Novacek	2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 April 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-31* is/are pending in the application.

4a) Of the above claim(s) *22-31* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *11/13/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This office action is in response to the Election filed April 27, 2005.

Election/Restrictions

Applicant's election of Group II, claims 1-21 in the Election filed April 27, 2005 is acknowledged. Applicant's election with traverse of claims 1-21 is acknowledged. The traversal is on the ground(s) that, allegedly, the subject matter of all claims 1-31 are sufficiently related. This is not found persuasive because the product as claimed in claims 22-31 can be made by another and materially different process than the method recited in claims 1-21. For example, the product recited in claims 22-31 can be made by selectively depositing the liner on certain areas of the substrate, instead of by non-selectively depositing the liner and then removing portions of the liner to leave the liner in selected areas, as is recited in the method of claims 1-21.

The requirement is still deemed proper and is therefore made FINAL.

Claims 22-31 are withdrawn from further consideration pursuant to 37 CFR 1.142(b), as being drawn to a nonelected invention, there being no allowable generic or linking claim. Applicant timely traversed the restriction (election) requirement in the reply filed on April 27, 2005.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this

subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-3, 7, 10, 13, 16 and 17 are rejected under 35 U.S.C. 102(e) as being anticipated by Lin et al. (US 6,743,669).

Regarding claim 1, Lin discloses providing a substrate (204) having a gate stack (210) on the surface of the substrate, forming an etch resistant liner (207) over the gate stack, forming a spacer (205) over the liner along sidewalls of the gate stack, removing the liner from regions of the substrate and gate stack not covered by the spacer, and leaving the liner in regions of the substrate and gate stack covered by the spacer, and forming a conductive material (230) in the regions of the substrate and gate stack not covered by the liner (Fig. 2A-2C; col. 5, ln. 6 – col. 6, ln. 67).

Regarding claim 2, Lin discloses, before forming the liner over the gate stack, providing a second gate stack (202) on the surface of the substrate (col. 5, ln. 11-17).

Regarding claim 3, Lin discloses forming the liner over the second gate stack, and forming the spacer over the liner along sidewalls of the second gate stack (Fig. 2A).

Regarding claim 7, Lin discloses that the gate stack (210) comprises a transistor gate stack and the second gate stack (202) comprises a resistor gate stack (Fig. 2C).

Regarding claim 10, Lin discloses, before forming the conductive material in the regions of the substrate and gate stack where the liner was removed, performing a preclean process on the surface of the substrate (col. 6, ln. 56-67).

Regarding claim 13, Lin discloses providing a substrate (204) having a first gate stack (210) and a second gate stack (202) on the surface of the substrate, forming a liner (207) over the first and second gate stacks, forming a spacer (205) over the liner and along the sidewalls of the first and second gate stacks, removing the liner from regions of the substrate and gate stacks not

covered by the spacer, forming a protective layer (206/208) over the second gate stack, and forming a conductive material (230) in the regions not covered by the liner (Fig. 2A-2C; col. 5, ln. 6 – col. 6, ln. 67).

Regarding claim 16, Lin discloses, before forming the conductive material, forming an insulative layer (206/208) over the second gate stack, and performing a preclean process on the substrate (col. 6, ln. 56-67).

Regarding claim 17, Lin discloses that the liner comprises an etch resistant material (col. 6, ln. 16-39).

Claims 1-3, 8, 11-13, 17, 18, 20 and 21 are rejected under 35 U.S.C. 102(b) as being anticipated by Shin et al. (US 20020037611).

Regarding claim 1, Shin discloses providing a substrate (10) having a gate stack (14/16) on the surface of the substrate, forming an etch resistant liner (20) over the gate stack, forming a spacer (24) over the liner along sidewalls of the gate stack, removing the liner from regions of the substrate and gate stack not covered by the spacer, and leaving the liner in regions of the substrate and gate stack covered by the spacer, and forming a conductive material (18/22) in the regions of the substrate and gate stack not covered by the liner (Fig. 3-4; para. 17-20).

Regarding claim 2, Shin discloses, before forming the liner over the gate stack, providing a second gate stack (14/16) on the surface of the substrate (Fig. 1).

Regarding claim 3, Shin discloses forming the liner over the second gate stack, and forming the spacer over the liner along sidewalls of the second gate stack (Fig. 1-3).

Regarding claims 8 and 18, Shin discloses that the liner can be made of aluminum oxide or tantalum oxide (para. 12).

Regarding claims 11 and 20, Shin discloses that the liner can be made of aluminum oxide or tantalum oxide, which inherently have a dielectric constant between 7 and 150 (para. 12).

Regarding claims 12 and 21, Shin discloses forming the conductive material, forming source and drain regions (not shown) within the substrate, wherein a location of the source and drain regions is determined by an end of the liner created by removing the liner from regions not covered by the spacer (para. 18).

Regarding claim 13, Shin discloses providing a substrate (10) having a first gate stack (14/16) and a second gate stack (14/16) on the surface of the substrate, forming a liner (20) over the first and second gate stacks, forming a spacer (24) over the liner and along the sidewalls of the first and second gate stacks, removing the liner from regions of the substrate and gate stacks not covered by the spacer, forming a protective layer (34) over the second gate stack, and forming a conductive material (18/22) in the regions not covered by the liner (Fig. 3-4; para. 17-20).

Regarding claim 17, Shin discloses that the liner comprises an etch resistant material (para. 12).

Claims 1-3, 6, 9, 13, 14, 17 and 19 are rejected under 35 U.S.C. 102(e) as being anticipated by Sugiyama et al. (US 6,800,909).

Regarding claim 1, Sugiyama discloses providing a substrate (1) having a gate stack (4/5/5a) on the surface of the substrate, forming an etch resistant liner (7) over the gate stack, forming a spacer (11) over the liner along sidewalls of the gate stack, removing the liner from regions of the substrate and gate stack not covered by the spacer, and leaving the liner in regions of the substrate and gate stack covered by the spacer, and forming a conductive material

(12a/12b) in the regions of the substrate and gate stack not covered by the liner (Fig. 8D-8L, 13A, 17A-17J; col. 8, ln. 59 – col. 12, ln. 51).

Regarding claim 2, Sugiyama discloses, before forming the liner over the gate stack, providing a second gate stack (4/5/5b) on the surface of the substrate (Fig. 13, 17A-17J).

Regarding claims 3 and 14, Sugiyama discloses forming the liner over the second gate stack, and forming the spacer over the liner along sidewalls of the second gate stack (Fig. 13A, 17J).

Regarding claim 6, Sugiyama discloses, before forming the liner over the gate stacks, forming a first spacer (6) along the sidewalls of the first and second gate stacks (col. 9, ln. 42-47).

Regarding claims 9 and 19, Sugiyama discloses that the liner can be made of SiC (col. 24, ln. 55-61).

Regarding claim 13, Sugiyama discloses providing a substrate (1) having a first gate stack (4/5/5a) and a second gate stack (4/5/5b) on the surface of the substrate, forming a liner (7) over the first and second gate stacks, forming a spacer (11) over the liner and along the sidewalls of the first and second gate stacks, removing the liner from regions of the substrate and gate stacks not covered by the spacer, forming a protective layer (13) over the second gate stack, and forming a conductive material (12a/12b) in the regions not covered by the liner (Fig. 8D-8L, 13A, 17A-17J; col. 8, ln. 59 – col. 12, ln. 51).

Regarding claim 17, Sugiyama discloses that the liner comprises an etch resistant material.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-5, 10, 13 and 15-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Krivokapic et al. (US 6,512,273) in view of Lin et al. (US 6,743,669).

Regarding claim 1, Krivokapic discloses providing a substrate (2) having a gate stack (8/10) on the surface of the substrate, forming an etch resistant liner (18) over the gate stack, forming a spacer (20) over the liner along sidewalls of the gate stack, removing the liner from regions of the substrate and gate stack not covered by the spacer, and leaving the liner in regions of the substrate and gate stack covered by the spacer (col. 4, ln. 38 – col. 5, ln. 40). Krivokapic discloses that the method of forming a semiconductor device "may then continue with standard CMOS processing including silicidation and metallization." (col. 5, ln. 37-40). But Krivokapic does not specifically disclose that the silicidation involves forming a conductive material in the regions of the substrate and gate stack not covered by the liner. Like Krivokapic, Lin discloses a process of forming a MOS transistor and siliciding regions of the transistor. Lin teaches that conventional CMOS silicidation involves forming a layer of conductive material on the exposed gate and source/drain regions of the transistor (col. 1, ln. 26-43). At the time of the invention, it would have been obvious to one of ordinary skill in the art to form conductive material in the regions of the substrate and gate stack not covered by the liner of Krivokapic because Krivokapic discloses using standard CMOS processing to silicide the transistor and, as is taught by Lin, standard CMOS silicidation processing involves forming conductive material in the exposed regions of the substrate and gate stack.

Regarding claim 2, Krivokapic discloses, before forming the liner over the gate stack, providing a second gate stack (8/10) on the surface of the substrate (Fig. 2A).

Regarding claim 3, Krivokapic discloses forming the liner over the second gate stack, and forming the spacer over the liner along sidewalls of the second gate stack (Fig. 2B).

Regarding claim 4, Krivokapic discloses, before removing the liner from regions of the substrate and gate stack not covered by the spacer, and leaving the liner in regions of the substrate and gate stack covered by the spacer, depositing a photoresist layer over the liner and the spacer of the second gate stack to prevent removal of the liner from the second gate stack (Fig. 2C; col. 5, ln. 4-6).

Regarding claim 5, Krivokapic discloses, after removing the liner from regions of the substrate and gate stack not covered by the spacer, and leaving the liner in regions of the substrate and gate stack covered by the spacer, forming an insulative layer (38/34) on the surface of the substrate that covers the second gate stack before forming the conductive material (col. 5, ln. 19-39).

Regarding claim 10, Krivokapic discloses that the method of forming a semiconductor device "may then continue with standard CMOS processing including silicidation and metallization." (col. 5, ln. 37-40). But Krivokapic does not specifically disclose that the silicidation involves performing a preclean process on the surface of the substrate. Like Krivokapic, Lin discloses a process of forming a MOS transistor and siliciding regions of the transistor. Lin teaches that conventional CMOS silicidation involves, before forming the conductive material in the regions of the substrate and gate stack where the liner was removed, performing a preclean process on the surface of the substrate (col. 6, ln. 56-67). Lin states, "A prerequisite for silicide formation is a silicon surface free of oxides." (col. 4, ln. 12-13). At the time of the invention, it would have been obvious to one of ordinary skill in the art to perform a

preclean process on the surface of the substrate of Krivokapic prior to the conductive material being deposited because Krivokapic discloses using standard CMOS processing to silicide the transistor and, as is taught by Lin, a preclean processing step to remove oxide from the substrate surface is a prerequisite of standard CMOS silicidation.

Regarding claim 13, Krivokapic discloses providing a substrate (2) having a first gate stack (8/10) and a second gate stack (8/10) on the surface of the substrate, forming a liner (18) over the first and second gate stacks, forming a spacer (20) over the liner and along the sidewalls of the first and second gate stacks, removing the liner from regions of the substrate and gate stacks not covered by the spacer, and forming a protective layer (30/38/34) over the second gate stack (col. 4, ln. 38 – col. 5, ln. 40). Krivokapic discloses that the method of forming a semiconductor device "may then continue with standard CMOS processing including silicidation and metallization." (col. 5, ln. 37-40). But Krivokapic does not specifically disclose that the silicidation involves forming a conductive material in the regions of the substrate and gate stack not covered by the liner. Like Krivokapic, Lin discloses a process of forming a MOS transistor and siliciding regions of the transistor. Lin teaches that conventional CMOS silicidation involves forming a layer of conductive material on the exposed gate and source/drain regions of the transistor (col. 1, ln. 26-43). At the time of the invention, it would have been obvious to one of ordinary skill in the art to form conductive material in the regions of the substrate and gate stack not covered by the liner of Krivokapic because Krivokapic discloses using standard CMOS processing to silicide the transistor and, as is taught by Lin, standard CMOS silicidation processing involves forming conductive material in the exposed regions of the substrate and gate stack.

Regarding claim 15, Krivokapic discloses, before removing the liner from regions of the substrate and gate stacks not covered by the spacer, depositing a photoresist layer over the liner

and the spacer of the second gate stack to prevent removal of the liner from the second gate stack (Fig. 2C; col. 5, ln. 3-6).

Regarding claim 16, Krivokapic discloses forming an insulative layer (30/38/34) over the second gate stack. Krivokapic discloses that the method of forming a semiconductor device "may then continue with standard CMOS processing including silicidation and metallization." (col. 5, ln. 37-40). But Krivokapic does not specifically disclose that the silicidation involves performing a preclean process on the surface of the substrate. Like Krivokapic, Lin discloses a process of forming a MOS transistor and siliciding regions of the transistor. Lin teaches that conventional CMOS silicidation involves, before forming the conductive material in the regions of the substrate and gate stack where the liner was removed, performing a preclean process on the surface of the substrate (col. 6, ln. 56-67). Lin states, "A prerequisite for silicide formation is a silicon surface free of oxides." (col. 4, ln. 12-13). At the time of the invention, it would have been obvious to one of ordinary skill in the art to perform a preclean process on the surface of the substrate of Krivokapic prior to the conductive material being deposited because Krivokapic discloses using standard CMOS processing to silicide the transistor and, as is taught by Lin, a preclean processing step to remove oxide from the substrate surface is a prerequisite of standard CMOS silicidation.

Regarding claim 17, Krivokapic discloses that the liner comprises an etch resistant material.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Christy L. Novacek whose telephone number is (571) 272-1839. The examiner can normally be reached on Monday-Thursday and alternate Fridays 7:30 - 5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amir Zarabian can be reached on (571) 272-1852. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

CLN
June 21, 2005

AMIR ZARABIAN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800